REMARKS

Claims 1, 2, 4-17 and 19-31 are pending and under consideration in the above-identified application. Claims 10 – 15 were withdrawn from consideration. Claims 3 and 18 were previously cancelled.

In the Office Action of March 5, 2008, Claims 1, 2, 4-17 and 19-31 were rejected.

In this Amendment, Claims 1, 16, 27 and 30 are amended, and Claims 10 – 15 are cancelled. No new matter has been introduced as a result of this Amendment.

Accordingly, Claims 1, 2, 4- 9, 16, 17 and 19-31 remain at issue.

I. 35 U.S.C. § 102 Anticipation Rejection of Claims

Claims 1, 2, 4-8, 16, 17, 19-23 and 27-31 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Fox* (U.S. Patent No. 6,566,697). Although Applicant respectfully traverses this rejection, Claims 1, 16, 27 and 30 were amended to clarify the invention and remove any ambiguities that may have been at the basis of this rejection.

In relevant part, each of independent Claims 1, 16, 27 and 30 now recites:

> "both a gate electrode of the drain transistor being turned-off and a gate electrode of the transfer electrode being turned-off are biased with a prescribed voltage to form the first conductivity type channel layer at an interface of a gate insulation film of each transistor."

The result of this recitation is that the formation of the first conductivity type channel layer leads to a suppression of a current flow from the photodiode. This is clearly unlike *Fox*.

Indeed, the result of this channel layer formation is described in at least paragraph [0085] of the specification (emphasis added):

[0085] This is because, by biasing the transfer gate electrode toward a negative voltage, a P-type channel is formed at the interface of a gate oxide film in the transfer gate part, thereby preventing a dark current from an interfacial level similarly to the buried PD.

It is submitted that Fox does not teach or suggest the formation of the first conductivity type channel layer. Accordingly, it is submitted that Claim 1 is patentable over Fox, as are dependent Claims 2, and 4-8.

As each independent Claims 16, 27 or 30 also recites the same distinguishable limitation as that of Claim 1, then each one of these claims is also patentable over *Fox*, as are its dependent claims, for at least the same reasons.

New Claims 32 and 33 are also patentable over *Fox*, since both of them also recite the same distinguishable limitation as that of Claim 1

Moreover, Claim 32 recites a simultaneously resetting of the floating diffusion parts on all the pixels in the imaging region section and simultaneously transferring of signal charges of the photodiodes on all the pixels to the floating diffusion parts.

As illustrated in FIG. 4 and disclosed in paragraph [0090] of the specification, a pulse in fed to the reset wirings 214A on all the rows, to reset the floating diffusions (FDs) 216 of all the pixels, and after that, a pulse is fed to the transfer wirings 211A on all the rows, to transfer the photoelectrons of the photodiodes (PDs) 219 of all the pixels to the FDs 216.

In contrast, *Fox* resets the FD 18 just after reading out (sampling) from the FD18 (See Fig. 4B). As such, one of ordinary skill in the pertinent art understands that the time lag between resetting a charge in the FD and transferring a charge to the FD leads to noise generation. That is, the charge made by incident outside light is accumulated during this time lag.

In addition, Claim 33 recites that the drain transistor is off during an operation to read out the signal charge of the floating diffusion part on a pixel row preceding the exposure start row.

As described in paragraph [0120] of the specification, during reading to the column signal processing circuit 230, the drain Tr 215 must be "off" even in a non-exposure time period. In case, the drain Tr 215 remained "on" during this non-exposure time period, there arises a slight difference in the output image between the signal which is output in a non-exposure time period and the signal which is output in a exposure time period, resulting in a generation of an horizontal line on the solid-state imaging device. In order to prevent this horizontal line generation, the drain TR 215 even in a non-exposure time period is turned off at least during the pixel output, and similarly in an exposure time period.

In contrast, *Fox* teaches that the drain Tr 22 is always on in a non-exposure time period because the exposure electronic control (EC) clock signal in FIG 4B is always high in that period.

Therefore, new Claims 32 and 33 are patentable over Fox for at least the above discussed respective distinguishable limitations.

Accordingly, Applicant respectfully requests that these claim rejections be withdrawn.

II. 35 U.S.C. § 103 Obviousness Rejection of Claims

Claims 9 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fox*. Applicant respectfully traverses this rejection.

Claims 2, 4-8, 16, 17, 19-23 and 27-31, which depend either directly or indirectly from Claims 1, 16, 27 and 30, shown above to be patentable over *Fox,* are also patentable for at least the same reasons.

Accordingly, Applicant respectfully requests that these claim rejections be withdrawn.

III. Conclusion

In view of the above amendments and remarks, Applicant submits that Claims 1, 2, 4- 9, 16, 17 and 19-31 are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

Dated: July 7, 2008 By:

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